REMARKS

Claims 1–22 are pending. Applicants respectfully traverse and request reconsideration and withdrawal of the rejections for the following reasons.

I. Summary of the Examiner's Objections/Rejections

Claims 1–10, 12–19 and 21-22 remain rejected under 35 U.S.C. § 103(a) over U.S. Patent Number 6,446,193 to Alidina et al. (Alidina), in view of Gregory T. Byrd, "Multithreaded Processor Architectures," IEEE SPECTRUM August 1995. Claims 11 and 20 are rejected under 35 U.S.C. § 103(a) over Alidina, in view of Byrd and in further view of U.S. Patent Number 5,673,377 to Berkaloff.

II. Applicants' Response to the Examiner's Rejections

The Applicants traverse the aforementioned claim rejections for at least the reasons set forth in greater detail below.

A. 35 U.S.C. § 103(a); Claims 1–10 and 12–19.

Claims 1–10 and 12–19 are rejected under 35 U.S.C. § 103(a) over Alidina, in view of Gregory T. Byrd, "Multithreaded Processor Architectures," IEEE SPECTRUM August 1995.

Alidina

Alidina is directed to reducing instruction cycles in a digital signal processor by processing two different register parts in a single processor cycle instead of two processor cycles. (Col. 2, lines 42–56.) Alidina teaches that repetitive operations can be carried out in *parallel*, so as to reduce the number of instructions and enhance the MIPs number by freeing up valuable instruction time for other operations. (Col. 3, lines 49–52.). (Emphasis added). Since multi-threading does not reduce the number of instructions or enhance total MIPs, Alidina teaches away from multi-threading. Instead, Alidina teaches that the data arithmetic unit comprises a power-efficient dual-MAC *parallel* pipelined structure particularly optimized for wireless and speech synthesis applications. (Col. 4, lines 23–25, emphasis added.) The Office Action acknowledges that Alidina teaches neither multi-threading nor having registers and operands that correspond to each individual thread. (Office Action, page 3, ref. #5.)

Byrd

Byrd is directed to multi-threaded processor architectures (Byrd, Title). Byrd teaches, in a multi-threaded architecture, threads are mapped onto hardware context, which each include general-purpose registers, status registers, and a program counter. (Byrd page 329 top insert.)

One context represents a running thread, while the others represent threads that are eligible to run or are waiting on an operation to complete. *Id.* Because of hardware limits, some threads are not currently mapped.

By and large, a multi-threaded processor's efficiencies are determined by four parameters: the number of contexts supported by the hardware; the cost of switching between contexts; the number of cycles typically executed between contexts switches, called the run length; and the characteristic lengthency of the operations that are to be hidden. (Byrd, page 40, third column.) If the number of contexts is increased but the other three parameters stay constant, then efficiency increases up to a point. *Id.* If there are too few contexts, then too few executable instructions will be on hand to cover for the long-lengthency operations. Eventually, though, the run-length and overhead for all of the contexts conceal lengthency completely and adding more contexts does not also add to efficiency.

The combination of Alidina and Byrd, to the extent Alidina and Byrd may be combined, would teach reducing instruction cycles in a digital signal processor by processing in parallel two different register parts in a single processor cycle, instead of two processor cycles, through storing contexts of multiple threads in multiple hardware registers.

Claim 1

Claim 1 recites:

> A multi-thread accumulation circuit that supports a plurality of threads, comprising:
>
> a first operation unit operatively coupled to receive a first operand and a second operand corresponding to an operation code issued by a selected thread of the plurality of threads, wherein the operation unit combines the first and second operands to produce a first operation result corresponding to the selected thread;
>
> a plurality of accumulation registers operatively coupled to the first operation unit, wherein each accumulation registry of the plurality of accumulation registers corresponds to one of the plurality of threads, wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread; and
>
> a selection block operably coupled to the plurality of accumulation registers and the first operation unit, wherein the selection block selects the second operand provided to the first

operation unit from a set of potential operands, wherein the set of potential operands includes contents of each accumulation register of the plurality of accumulation registers.

NEITHER ALIDINA NOR BYRD TEACHES AT LEAST "WHEREIN A SELECTED ACCUMULATION REGISTER THAT CORRESPONDS TO THE SELECTED THREAD STORES THE FIRST OPERATION RESULT CORRESPONDING TO THE SELECTED THREAD"

To establish a *prima facie* case of obviousness, each and every element arranged, as required by the claims, must be taught or suggested in the prior art. M.P.E.P. 2143.03.

The Office Action fails to establish a *prima facie* case of obviousness because the Office Action fails to show how each and every element in the claims is taught by the references. Among other things, the Office Action fails to show where the combination of Alidina and Byrd teach "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread." According to the Office Action "Alidina has taught a digital signal processor specializing in scientific calculations. (Alidina, col. 1, lines 17-28). Also, according to the Office Action, Byrd has taught multi-threading and having registers in operands that correspond to each individual thread. (Byrd pages 38-40.) However, the Office Action does not show specifically where Byrd teaches a thread as arranged in the claims. Further, the Office Action fails to show how Byrd, as cited, teaches "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread." Therefore, the combination of Alidina, in view of Byrd, as cited, fails to teach, and further teaches away from, among other things, "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread" as arranged in the claims. Consequently, for at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness.

The Office Action asserts that Alidina, at column 1, line 64 to column 2, line 5, describes "wherein a selected accumulation register [that corresponds to the selected thread] stores the first operation result [corresponding to the selected thread]." By omitting limitations when quoting the claims, the Office Action acknowledges that Alidina does not describe each and every element in the claims, including "wherein selected accumulation register that corresponds to the selected thread" and "stores the first operation result corresponding to the selected thread."" As a result, the Office Action, based on its selective quotation of claim 1 on page 2, paragraph 4

letter B, acknowledges that Alidina does not describe "wherein each accumulation register of the plurality of the accumulation registers corresponds to one of the plurality of threads," and "wherein a selected accumulation register that corresponds to the selected threads stores the first operation result corresponding to the selected thread."

Further, the Office Action acknowledges, based on the quotation of claim 1 on page 2, paragraph 4(a), by omitting language from the claim, Alidina fails to describe "a second operand corresponding to an operation code issued by a selected thread of the plurality of threads" and "wherein the operation unit combines the first and second operands to produce a first operation result corresponding to the selected thread."

As a result, since the function and the structure of a thread is not disclosed at all in Alidina, multiple limitations related to the thread cited in the claims are also not described in Alidina. Further, the Office Action fails to show how Byrd, as cited, teaches "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread." Therefore, the combination of Alidina, in view of Byrd, as cited, fails to teach, and further teaches away from, among other things, "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread" as arranged in the claims. Consequently, the Office Action fails to establish a *prima facie* case of obviousness. As such, the Office Action ignores explicit limitations in the claims.

There is no motivation to combine Alidina with Byrd because Alidina teaches away from the claims since, as previously stated, Alidina teaches avoiding multi-threaded context switching Alidina teaches "repetitive operations that can be carried out in parallel, so as to reduce the number of instructions typically enhance the number of MIPS. . . ." Since Alidina is directed to processing two different register parts in a single processor cycle for speech coding, Alidina, is directed to a problem different from that addressed in the claims. (Col. 2, lines 42–56.)

Despite the explicit teachings of Alidina described above, the Office Action at paragraph 5 asserts that "A person of ordinary skill in the art and as taught in Byrd would recognize that multi-threading is best suited for scientific and engineering programs" (Byrd page 38) and "increases the speed and efficiency in the processor by allowing the processor to run other procedures while waiting for [a] longer background operations, such as accessing slower memory, to complete" (Byrd pages 38-40.) However, for at least the reasons shown

above, this assertion is unsupported and is contrary to the explicit teachings of Byrd. As a result, there is no motivation to combine the references, since Alidina teaches away from the claims. Consequently, the Office Action fails to establish a *prima facie* case of obviousness.

As previously stated, to the extent Alidina and Byrd may be combined, such a combination would teach reducing instruction cycles in a digital signal processor by parallel processing two different register parts in parallel in a single processor cycle, instead of two processor cycles, through storing contexts of multiple threads in multiple hardware registers. As a result, the combination of Alidina and Byrd is directed to solving a problem completely different from that addressed in the claims. Therefore, the combination of Alidina, in view of Byrd, as cited, teaches away from the claims, namely process-swapping, and fails to teach each and every element as arranged in the claims. Consequently, the Office Action fails to establish a *prima facie* case of obviousness.

The modification of Alidina, in view of the cited suggestion of Byrd, would change the principle of operation of Alidina because Alidina teaches "repetitive operations that can be carried out in *parallel* so as to reduce the number of instructions and enhance MIPs. . . ." (Alidina, col. 3, lines 49-52; see col. 4, lines 21-25, emphasis added.) Instead of multi-threaded processing as claimed, Alidina teaches an opposite approach: executing repetitive instruction in parallel. Therefore, the modification suggested by Byrd, if possible, would change the principle of operation of the claimed invention because Alidina, as cited, (1) teaches executing repetitive instructions in parallel, (2) teaches enhancing MIPs by parallel processing and (3) teaches processing in a single instruction cycle to effect efficient loading or storing operations and therefore teaches against saving and restoring registers.[1] (Col. 2, lines 14–65.) Consequently, for at least these reasons, there is no motivation to combine the references and, therefore, the Office Action fails to establish a *prima facie* case of obviousness.

[1] If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (CCPA 1959). See M.P.E.P. 2143.01.

THE COMBINATION OF ALIDINA AND BYRD FAILS TO TEACH AT LEAST "A SELECTION BLOCK OPERABLY COUPLED TO THE PLURALITY OF ACCUMULATION REGISTERS AND THE FIRST OPERATION UNIT, WHEREIN THE SELECTION BLOCK SELECTS THE SECOND OPERAND PROVIDED TO THE FIRST OPERATION UNIT FROM A SET OF POTENTIAL OPERANDS, WHEREIN THE SET OF POTENTIAL OPERANDS INCLUDES CONTENTS OF EACH ACCUMULATION REGISTER OF THE PLURALITY OF ACCUMULATION REGISTERS"

As previously stated, the Office Action acknowledges that Alidina does not describe "multi-threading and having registers and operands which correspond to each individual thread." Accordingly, Alidina also fails to teach "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread.

The cited portion of Alidina at paragraph 4, lines 63 through 66, which states, "The modified results from the respective saturators SAT1, SAT2 and SAT3 are then fed through a split multi-plexer SMUX to a register array 50 comprising eight 40-bit accumulators a0 through a7" is limited to modifying results from saturators SAT1, SAT2 and SAT3 and then feeding through split multi-plexer SMUX to a register array 50 rather than "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread."

According to the Office Action in paragraph 35, "As for the path, which passes through other blocks, the claim language states 'comprising' which is open," and, "As long as the elements recited in the claim are taught in the reference, the extraneous elements do not matter." However, in order to show that Alidina teaches "wherein the selection block selects the second operand provided to the first operation unit from a set of potential operands," the Office Action must show where Alidina teaches all the limitations as arranged in the claims, including, among other things, the claimed routing. Therefore, since the Office Action fails to show where Alidina teaches the specific routing, namely "wherein the selection block selects the second operand provided to the first operation unit from a set of potential operands," the Office Action fails to show where either Alidina or Byrd in combination teaches all of the elements as arranged in the claim. Nevertheless, the path, as asserted in the Office Action, passes through other blocks and, therefore, some teaching must be shown for routing the signal through only those blocks out of the many blocks in order to form the specific path. FIG. 3 fails to show the specific routing path

and, further, fails to show the required control signals to establish any such path, as asserted in the Office Action. As a result, the combination of Alidina and Byrd fails to teach "a selection block operably coupled to the plurality of accumulation registers and the first operation unit, wherein the selection block selects the second operand provided to the first operation unit from a set of potential operands, wherein the set of potential operands includes contents of each accumulation register of the plurality of accumulation registers." (*See* Alidina, col. 4, lines 57-59.)

FIG. 3 of Alidina teaches performing arithmetic functions rather than a multi-thread process and, therefore, solves a problem different from that addressed in the instant application. Consequently, the extra functional blocks for performing the arithmetic functions beyond those needed for performing process-swapping in the multi-thread environment would add unnecessary expense and complexity and would hinder performance in a multi-thread environment because of the unnecessary hardware and processing. Accordingly, the complex arithmetic unit taught by Alidina actually teaches away from the claimed invention because the added complexity and the resultant reduction of speed and performance would not be suitable for performing time-sensitive operations, such as process-swapping in a multi-thread environment. Furthermore, modifying the arithmetic logic unit in Alidina, as suggested in the Office Action, to perform process-swapping in a multi-thread environment would require the elimination of the arithmetic functions, thus rendering Alidina unsatisfactory for its intended purpose as an arithmetic unit, since the arithmetic unit would need to be removed to achieve the performance requirements for process-swapping.[2] Nevertheless, the Office Action at paragraph 37 states that the Examiner "is unsure how this argument is related to the claim language and related to the invention." As previously stated, since Alidina teaches an arithmetic logic unit, such an arithmetic logic unit performs arithmetic functions, rather than performing multi-threaded processes, as previously stated. The Applicants would like to point out the distinction between an arithmetic logic unit performing arithmetic functions and multi-threaded operations such as process-swapping.

The Office Action asserts that the SMUX, as cited in Alidina, is the claimed selection block. However, as shown above, Alidina does not teach a path from the control registers via the

[2] If the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 200, 221 U.S.P.Q. 1125 (Fed. Cir. 1984); M.P.E.P. 2143.02.

SMUX to the first operation unit (no equivalent element in Alidina is identified in the Office Action), but rather the XYFB couples SMUX to the register X(32). In Alidina, "the eight accumulators are controlled according to modes defined by preselected mode bits provided by control registers auc0 and auc1 to selectively provide feedback along a feedback path XYFBK to the x-y multiplier registers x(32) and y(32)." (Col. 5, lines 13–17.) If the rejection is maintained, and the registers x(32) in Alidina are equated to the first operation unit rather than the accumulation registers, then Alidina fails to teach at least "wherein the operation unit combines the first and second operands to produce a first operation result corresponding to the selected thread," as claimed. As a result, Alidina does not teach, and Applicants request a showing of, "wherein the selection block selects the second operand provided to the first operation unit from a set of potential operands, wherein the set of potential operands includes contents of each accumulation register of the plurality of accumulation registers." Therefore, for at least these reasons, the combination of Alidina, in view of Byrd, as cited, fails to teach each and every element as arranged in the claims. Consequently, the Office Action fails to establish a *prima facie* case of obviousness.

NEITHER ALIDINA NOR WILSON TEACHES AT LEAST "A FIRST OPERATION UNIT OPERABLY COUPLED TO RECEIVE A FIRST OPERAND AND A SECOND OPERAND CORRESPONDING TO AN OPERATION CODE ISSUED BY A SELECTED THREAD OF THE PLURALITY OF THREADS, WHEREIN THE OPERATION UNIT COMBINES THE FIRST AND SECOND OPERANDS TO PRODUCE A FIRST OPERATION RESULT CORRESPONDING TO THE SELECTED THREAD"

The Office Action cites Alidina (abstract, lines 1-4; col. 2, lines 46-48; col. 4-5, lines 26-27; Fig. 3) for teaching "a first operation unit operably coupled to receive a first operand and a second operand corresponding to an operation code issued by a selected thread of the plurality of threads." However, as stated in the previous response, this general reference to over 70 lines in a reference without showing equivalent claim elements does not make apparent, or explain with specificity, how each claim is rejected. M.P.E.P. 706, C.F.R. § 1.104(c)(2). For example, Applicants are unable to find any reference in Alidina, as cited, "corresponding to an operation code issued by a selected thread of the plurality of threads," as claimed. As previously stated, Applicants cannot find where Alidina teaches multi-threaded processing.

According to the Office Action at paragraph 38, "Alidina was relied upon to teach multi-threading." As previously stated, Alidina explicitly teaches away from a multi-threaded accumulation circuit, since Alidina teaches "it is desirable to avoid the overhead costs of

process-swapping," and "multi-threaded context switching can be quite expensive, since there may be many registers to save and restore." Despite the explicit language in Alidina that teaches away from multi-threaded processing, the Examiner continues to ignore these explicit teachings and persists instead to assert that "Alidina was relied upon to teach multi-threading." (Office Action ¶ 38.) To the extent Alidina and Alidina may be combined, such a combination would teach reducing instruction cycles in a digital signal processor by processing two different register parts in parallel in a single processor cycle instead of two swapped threaded processor cycles. Consequently, among other things, the combination of Alidina, in view of Alidina, as cited, fails to teach, and Applicants request a showing of, "a first operation unit operably coupled to receive a first operand and a second operand corresponding to an operation code issued by a selected thread of the plurality of threads." Therefore, the combination of Alidina, in view of Alidina, as cited, fails to teach each and every element as arranged in the claims. Consequently, the Office Action fails to establish a *prima facie* case of obviousness.

The Office Action fails to indicate, and Applicants are unable to find, any reference to where Alidina or Alidina, in combination or individually, as cited, teaches "wherein the operation unit combines the first and second operands to produce a first operation result corresponding to the selected thread." Since the combination of Alidina and Byrd fails to describe multi-threading and process-swapping, as previously described, the combination of Alidina and Byrd fails to describe a "selected thread." Consequently, the combination of Alidina and Byrd teaches against "wherein the operation unit combines the first and second operands to produce a first operation result corresponding to the selected thread." Again, if the Examiner maintains this rejection, Applicants again respectfully request a showing in Alidina and Byrd of each and every element arranged as claimed.

As to claim 2, the Office Action cites Alidina as teaching a control block, as claimed. However, the cited portion of Alidina instead describes bus-accessible control registers rather than "a control block operably coupled to the selection block and the plurality of accumulation registers, wherein the control block receives information based on the operation code and generates control information provided to the plurality of accumulation registers and the selection block, wherein the control information provided to the plurality of accumulation registers causes the selected accumulation register to store the result corresponding to the selected thread when the operation code corresponds to an accumulate operation." The Office

Action fails to show how Alidina teaches that the bus-accessible control registers are equivalent to the control block as claimed and, therefore, fails to establish a *prima facie* case of obviousness. Applicants at least reassert that the references do not teach each and every element, as arranged in the claims with respect to claim 1. Claim 2 adds additional novel and nonobvious subject matter for at least these reasons and is also allowable, at least, as depending from an allowable base claim.

As to claims 3-6, 8-10, 12-16 and 18-19, Applicants at least reassert the above reasons. Each claim adds additional novel and nonobvious subject matter and is allowable at least as depending from an allowable base claim. Further, the combined references do not teach each and every element as arranged in the claims.

As to claims 7 and 17, the cited portion of Byrd, rather than teaching an arbitration module, as asserted in the Office Action, teaches against arbitration in a multi-threaded processor, since Byrd as cited on page 39 teaches "waiting on an operation to complete." Accordingly, the assertion that it is inherent, and that there must be a unit as claimed, is improper. A supporting reference is respectfully requested if the rejection is maintained. The Office Action acknowledges that Alidina does not teach multi-threading and having registers and operands that correspond to each individual thread. Further, the Office Action, on page 12, paragraph 26, and page 13, paragraph 14 acknowledges that Alidina fails to teach an arbitration module that receives command codes corresponding to a plurality of threads, wherein at least a portion of the command codes correspond to a plurality of threads, wherein at least a portion of the command codes correspond to multiply and accumulate operations and wherein the arbitration module determines an order of execution of the command codes. Applicants also at least reassert the above statements, *inter alia*, and that the references do not teach each and every element as arranged in the claims with respect to claim 1. Claims 7 and 17 add additional novel and nonobvious subject matter and are also allowable, at least as depending from an allowable base claim.

B. 35 U.S.C. § 103(a); Claims 11 and 20.

Claims 11 and 20 are rejected under 35 U.S.C. § 103(a) over Alidina in view of Byrd, and in further view of U.S. Patent Number 5,673,377 to Berkaloff. The Office Action acknowledges that Alidina does not teach multi-threading and having registers and operands that correspond to each individual thread. The Office Action also acknowledges that Alidina does

not teach wherein the first register section accumulates diffuse color information corresponding to graphics primitives, and wherein the second register section accumulates specular color information corresponding to the graphics and primitives. Further, the motivation provided in the Office Action to combine the references, which states, "because it is needed in the calculations to create effective images," provides no basis for the meaning of "effective images," and further uses circular reasoning, and therefore fails to establish motivation to combine the references. Claims 11 and 20 add additional novel and nonobvious subject matter and are also allowable at least for the above reasons and as depending from an allowable base claim.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

By _____
Themi Anagnos
Reg. No. 47,388

Dated: August 9, 2004

Vedder, Price, Kaufman & Kammholz, P.C.
222 North LaSalle Street
Chicago, Illinois 60601
PHONE: (312) 609-7970
FAX: (312) 609-5005

CHICAGO/#1259616.1